CLAIMS

1. An active matrix array device comprising an array of individually addressable matrix elements, first and second sets of crossing address conductors connected to the matrix elements, the array of matrix elements and the sets of address conductors being carried on a substrate, and an addressing circuit connected to the sets of row and column conductors for addressing the matrix elements which addressing circuit comprises a multiplexing circuit integrated on the substrate and connected to the first set of conductors and having a plurality, n, of signal bus lines, the address conductors of the first set being arranged in a series of groups with each group comprising n successive address conductors and the multiplexing circuit being arranged to couple sequentially each group of address conductors to the signal bus lines with each address conductor in a group being coupled to a respective one of the bus lines, the addressing circuit further including a respective signal processing circuit connected to each bus line, characterised in that the signal processing circuits associated with the bus lines are integrated as respective circuit blocks on the device substrate with the individual signal processing circuit blocks associated with adjacent column conductors being located close together on the device substrate.

2. An active matrix array device according to Claim 1, characterised in that the order in which the signal processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected.

3. An active matrix array device according to Claim 2, characterised in that the multiplexing circuit extends alongside one edge of the array of matrix elements and the signal processing circuit blocks are arranged in at least one row extending alongside the multiplexing circuit.

4. An active matrix array device according to Claim 1, Claim 2 or Claim 3, characterised in that the matrix elements comprise electro-optic display elements.

5. An active matrix array device according to Claim 4, characterised in that the signal processing circuits comprise digital to analogue converter circuits.

6. An active matrix array device according to Claim 4, characterised in that the signal processing circuits comprise sample and hold circuits.

7. An active matrix array device according to Claim 1, Claim 2 or Claim 3, characterised in that the matrix elements comprise sensing elements each responsive to an input to produce an output signal along its associated address conductor of the first set.

8. An active matrix array device according to Claim 7, characterised in that the signal processing circuits comprise sense amplifier circuits.